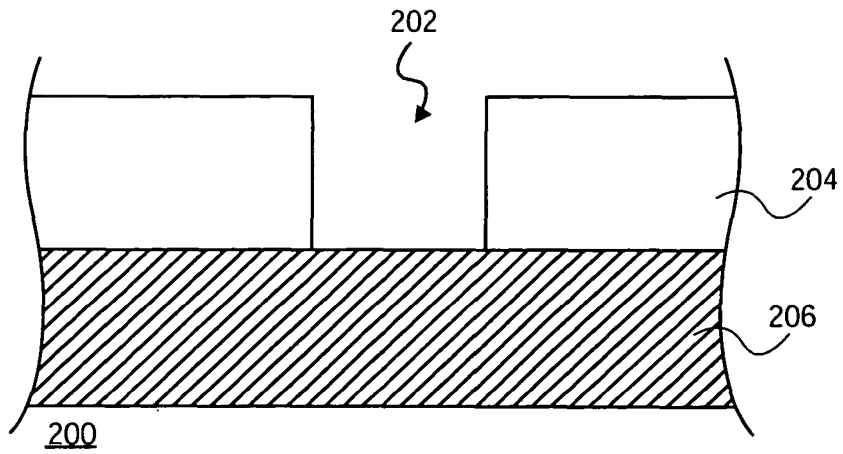
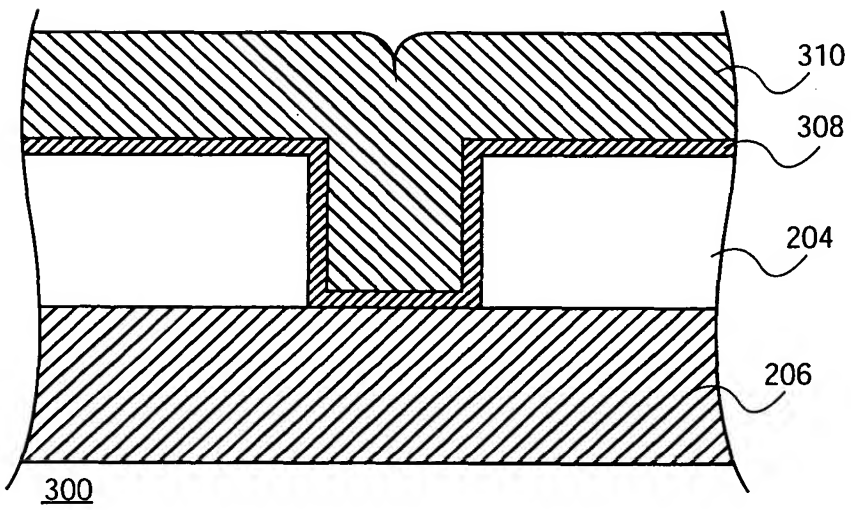


A cross-sectional view of a semiconductor device 100. The device features a substrate 108 with a well 108 formed in it. A layer 102 is disposed on the substrate 108. A layer 104 is disposed on top of layer 102. A layer 106 is disposed on top of layer 104. A layer 110 is disposed on top of layer 106. A layer 112 is disposed on top of layer 110. A layer 114 is disposed on top of layer 112. A layer 116 is disposed on top of layer 114. A layer 102 is also disposed on top of layer 106. A layer 104 is also disposed on top of layer 106. A layer 106 is also disposed on top of layer 106. A layer 110 is also disposed on top of layer 106. A layer 112 is also disposed on top of layer 106. A layer 114 is also disposed on top of layer 106. A layer 116 is also disposed on top of layer 106.

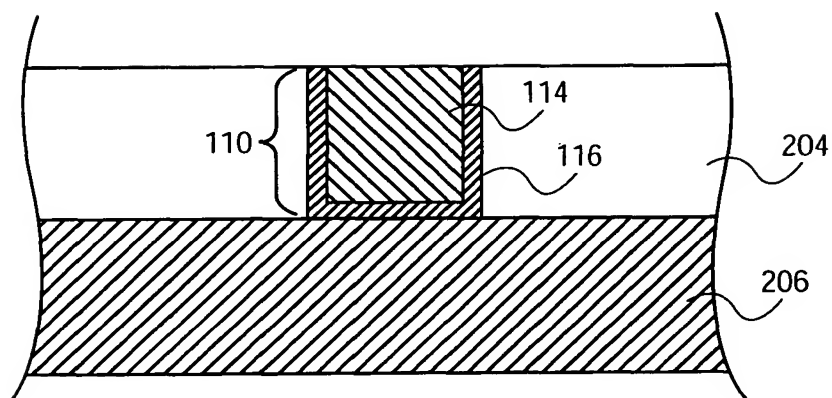
**FIG. 1**  
**(PRIOR ART)**



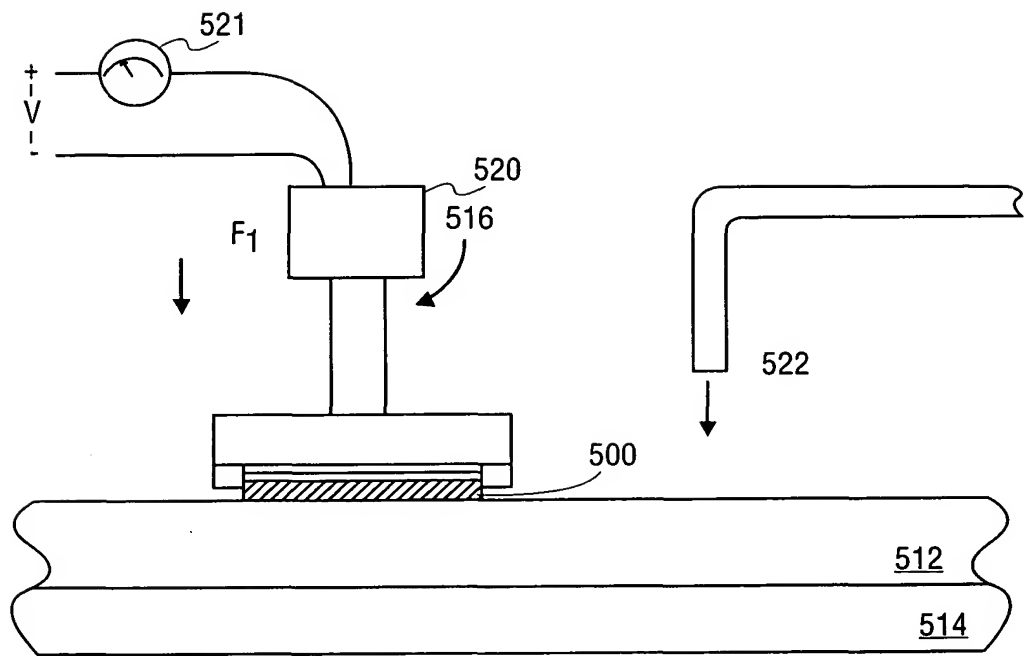
**FIG. 2**  
(PRIOR ART)



**FIG. 3**  
(PRIOR ART)

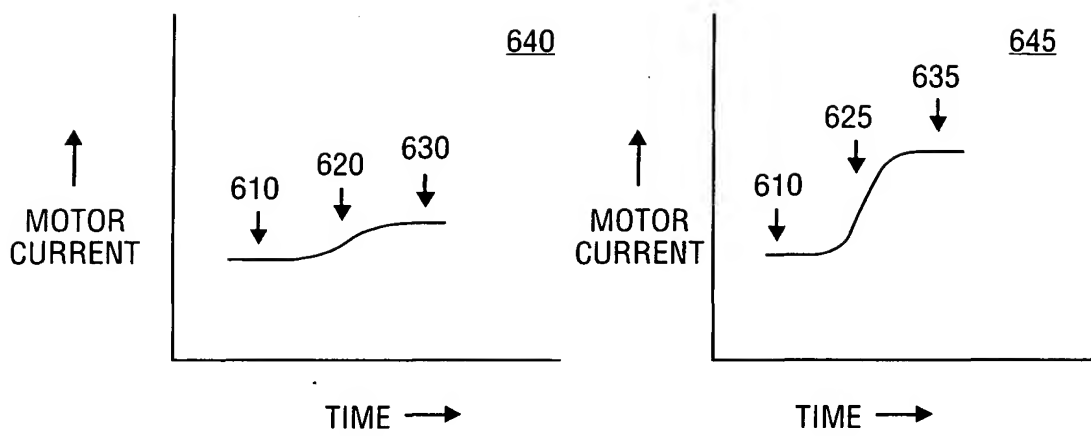


**FIG. 4**  
(PRIOR ART)



**FIG. 5**

**Abstract**



**FIG. 6**

REMOVING EXCESS VIA MATERIAL FROM  
AN INTEGRATED CIRCUIT WAFER  
BY CHEMICAL MECHANICAL POLISHING  
THE WAFER WITH A SLURRY AND AN  
OXIDATION AGENT FOR THE VIA  
MATERIAL ON A SURFACE  
710



MONITORING THE CURRENT REQUIRED TO  
ROTATE THE WAFER ON THE SURFACE AS  
A MEASURE OF THE EXCESS VIA  
MATERIAL REMOVAL ENDPOINT  
720



OPTIMIZING THE ENDPOINT SIGNAL BY  
BUFFERING A SLURRY USED IN THE  
CHEMICAL MECHANICAL POLISH  
730

**FIG. 7**